Time Interval Measurement Based on Fine-Time Synthesis Module

Guoqing Sun[1], Zhaohui Wang[1], Jiameng Dong[1], Song Yu[1], Xing Chen[1], Bin Luo[1,*]

[1]State Key Laboratory of Information Photonics and Optical Communications, School of Electronic Engineering, Beijing University of Posts and Telecommunications, Beijing, China

Email: luobin@bupt.edu.cn

The time-to-digital converter (TDC) is a key technology for achieving accurate time delay measurements in fiber-optic time transmission and synchronization system[1]. Current architectures for TDC implementation mainly consist of coarse counters paired with different fine counter architectures[2]. These architectures include multi-phase clocked counters[3] and multi-chain parallel structures[4]. Here, we propose and implement a new fine counter architecture that synthesizes the time interval between pulses and the reference clock into a single pulse. The width of synthesized pulse is measured to enhance precision through the reuse of measurement units.

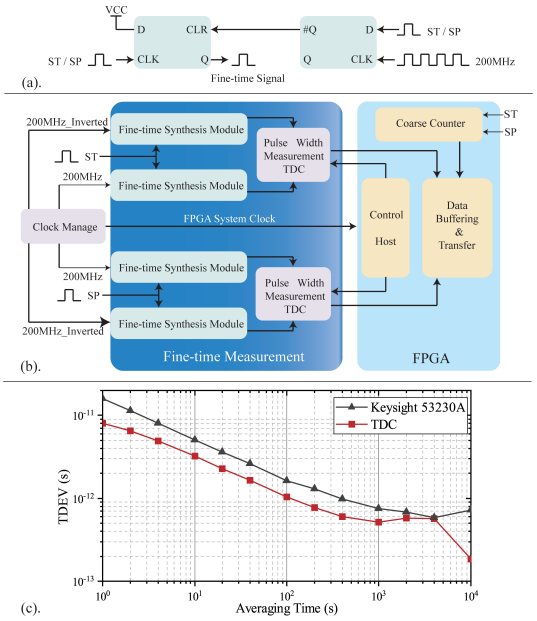

Fig. 1: (a). Principle of fine-time synthesis module (b). Diagram of overall system. (c). The TDEV of TDC and Keysight 53230A

Fig. 1(a) illustrates the principle of the fine time synthesis module. This paper proposes connecting the clock signal, start signal (ST), or stop signal (SP) through the different inputs of two D flip-flops to obtain the fine time signal. Fig. 1(b) depicts the diagram of overall system. The inverted clock signals provided by the time management module are used to overcome the dead zone problem. And the measurements of the fine time between ST/SP and inverted clocks improve the measurement precision through averaging. The TDC stability is evaluated through the back-to-back (BTB) experiment. The 1PPS (one pulse per second) from the pulse generator (SRS DG645) is divided and input into the ST and SP channels of TDC. Meanwhile, a commercial time interval counter (Keysight 53230A) is used for measurement as a comparison. The measurement results are shown in Fig. 1(c). The short-term TDEV is equal to 8.07 ps@1s, and the long-term TDEV is equal to 0.18 ps@10^4s. Additionally, the proposed TDC is applied in a laboratory-built round-trip time synchronization system over 680km fiber link. The standard deviation of the system is measured to be 38.02ps.

[1] Wang, J et al., "Fiber-optic joint time and frequency transfer with the same wavelength," Opt. Lett. 45, 208-211, 2020.

[2] S. Tancock et al., "A Review of New Time-to-Digital Conversion Techniques," in IEEE Trans Instrum Meas, vol. 68, no. 10, pp. 3406-3417, 2019.

[3] Mao, X et al., "A Low Temperature Coefficient Time-to-Digital Converter with 1.3 ps Resolution Implemented in a 28 nm FPGA." *Sensors (Basel, Switzerland)* vol. 22,6 2306. 16 Mar. 2022.

[4] X. Yu et al., "A Low-Cost FPGA-Based Coarse-Fine Counting Time-to-Digital Converter With External High-Precision Reference Clock," in IEEE Trans Instrum Meas, vol. 72, pp. 1-10, 2023.